

# The Parallel Series

G Thomas

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nc n xn n n 1 s n 1 s 0 init p 0 load a  
and b repeat m times

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bit concatenation to form the input bits  
wire 3 0 a wire 3 0 b case a b endcase  
and your case statement will have 256  
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verilog the inputs are clk clock rst reset  
a 8 bit multiplier b 8 bit multiplicand  
and the outputs are p product and rdy  
ready signal indicating multiplication is  
over

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web you cannot use the multiplication  
operator of verilog the lab file  
submission deadline is on 9 28 by 6  
00pm write simulation for a multiplier  
the input output ports of the 8 bit  
multiplier is as follows module  
seqmultiplier input wire clk input wire  
enable input wire 7 0 a input wire 7 0 b  
output wire 15 0 c

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