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LL Leslie

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endmodule i thought of the following test module
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web truth table the binary multiplier truth table is given
below binary multiplier types the following are the binary
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web nov 26 2021 bits bits 1 a in reg a in reg 1 b in reg b in
reg 1 end endcase if bits 0 begin display multiplication
completed finish reg 1 b1 conversion of binary to bcd for i 0 i
n 2 i i 1 begin if 3 n 2 3 1 4 1 bcd reg 3 0 5 bcd reg 3 0 bcd
reg 3 0 3 if 7

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simulates 4 bit multiplier without using multiplication need
just to use half and full adders so i succeeded to program the
solution from some instance this is the code module ha sout
cout a b output sout cout input a b assign sout a b assign
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multiplier is as follows module seqmultiplier input wire clk

input wire enable input wire 7 0 a input wire 7 0 b output
wire 15 0 c